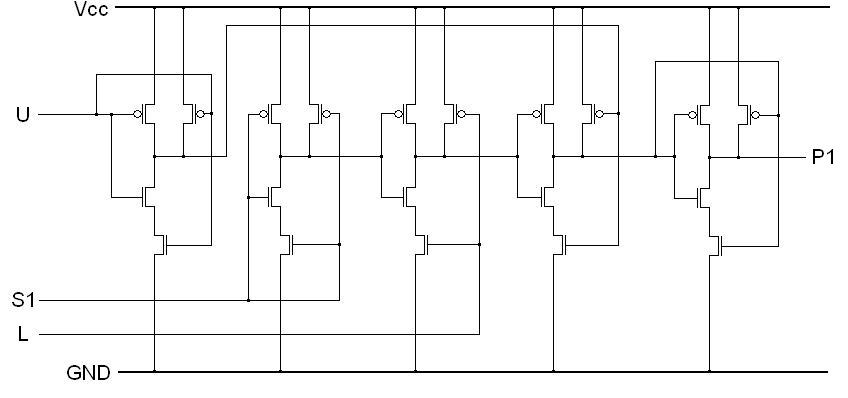
**Part 1: SSI-Logic Implementation of a Boolean Logic Equation with NAND2 gates**

Equation for pump P1:

When the water level goes more than 90% (U=0), pump P1 must stop regardless of the condition of the other 2 sensors S1 and L. If the level is under 90% (U=1) and either the water is clear (S1=1) or the level is also under 50 % (L=0) or both of them at the same time, the pump P1 pumps water into the tank (P1=1)

P1 = ¬U ^ (¬L v S1)

Controller is built with NAND2 gates (74HC00) for output P1 of the settling tank. Switches are used to mimic the sensor inputs and LED is visualizing the value of the output. Results of testing and the circuit are given below.



Truth table of expected and actual results:

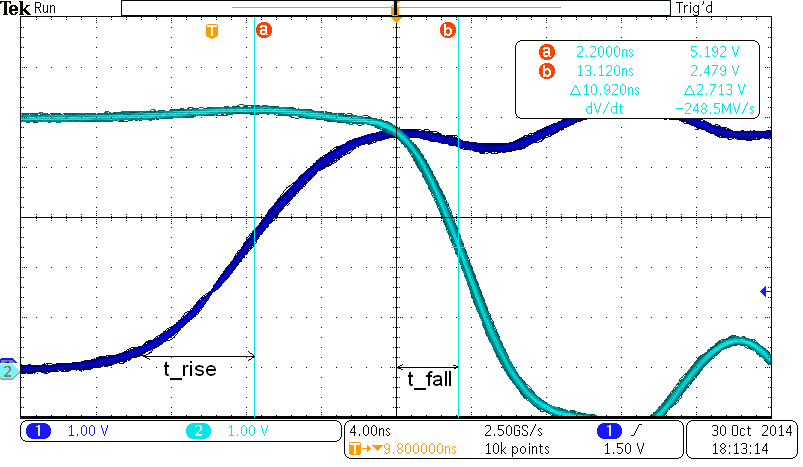
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| U | L | S1 | P1(expected) | P1(experiment) |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 |

**Part 2: Measurement of the propagation delay of digital devices.**

**LAB TASK 2.1: Measurement of the delay of a single NAND2 gate (74HC00)**

The measurement of the propagation delay is done with the help of a function generator and an oscilloscope. A termination resistor is used in parallel with the circuit that reduces the voltage applied with a factor of 2. That is why the voltage displayed on the generator is twice as much as the voltage measured by the oscilloscope and applied on the input of the NAND2 gate. Apart from that a 5V offset is added to the function generator output voltage to avoid negative voltages to be applied to the CMOS inputs. So it is ensured that the input voltage to the circuit was in the range 0...5V.

As the output of the NAND2 gate varies with every change of level of the input U, the function generator is connected to that input and a rectangular input signal at 1MHz frequency is applied. The second input is connected to ground. Then the propagation delay for a single gate is measured with the oscilloscope.



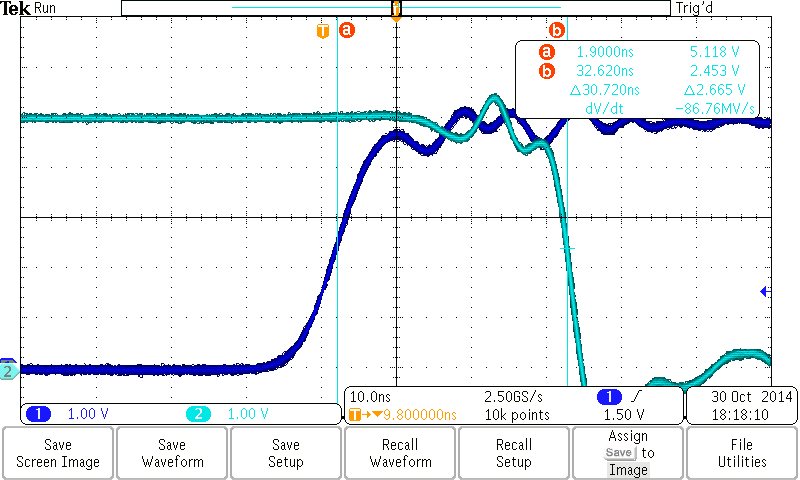
Propagation delay of a single NAND2 gate is: **∆t = 10.92 ns**

It is obvious from the screenshot that the delay for falling and rising edges is not identical:

4 ns per unit: **t\_rise ≈ 6 ns; t\_fall ≈ 3.5 ns**

**LAB TASK 2.2: Measurement of the delay of the whole circuit.**

As it can be seen from the schematics from task 1, the signal U passes through 3 NAND2 gates. Therefore the expected delay of the whole circuit is expected to be 3 times bigger than that for the single NAND2 gate. (≈30 ns)

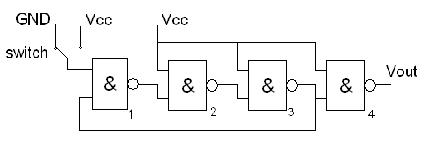


Propagation delay for the whole tank controller is: **∆t = 30.72 ns**

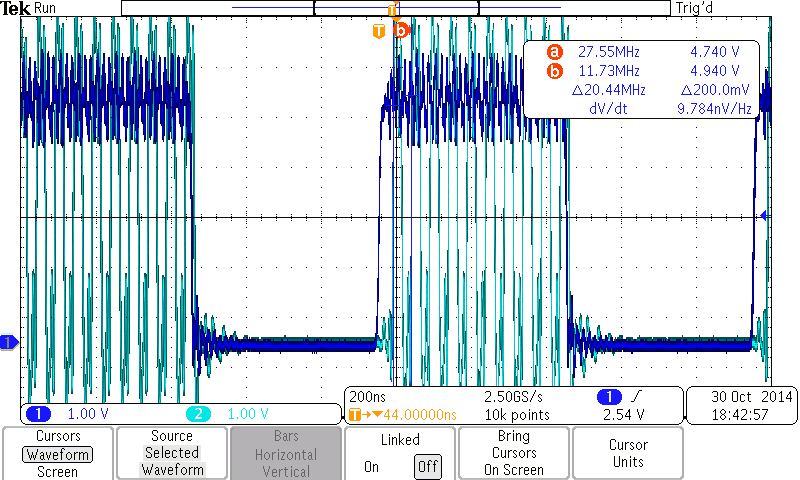
The result obtained is similar with the one expected!

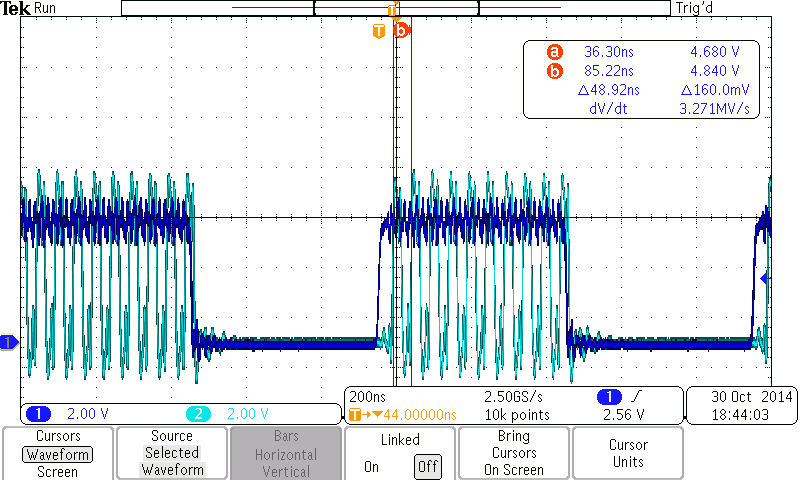
**Part 3: Combinational loops.**

**LAB TASK 3.1** The point of this task is to understand how feedback loops work and what side effects can happen when improperly inserted.



The circuit given is implemented using a 74HC00 device and a debounced push button for the switch. The oscilloscope (Channel 2) is connected to the output of the fourth NAND gate and Vout is being measured. (Channel 1 shows the input signal Vcc) When the switch is connected to ground, Vout is 0V and remains unchanged in time. When the switch is connected to Vcc the output results in oscillations and Vout changes between low and high every loop. The frequency and the delay for each loop are then measured.





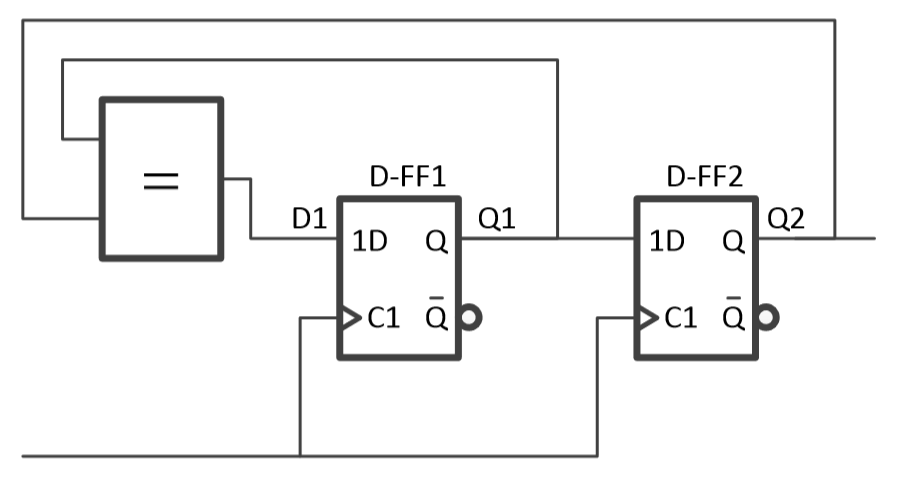
**f = 20.44 MHz; ∆t = 48.92 ns**

Compared with the results obtained in task 2.1 those measurements seem to be valid. The delay for a single gate was measured to be **10.92 ns** so the expected delay for all the 4 NAND gates of the given circuit is expected to be **4x11 ≈ 44 ns**

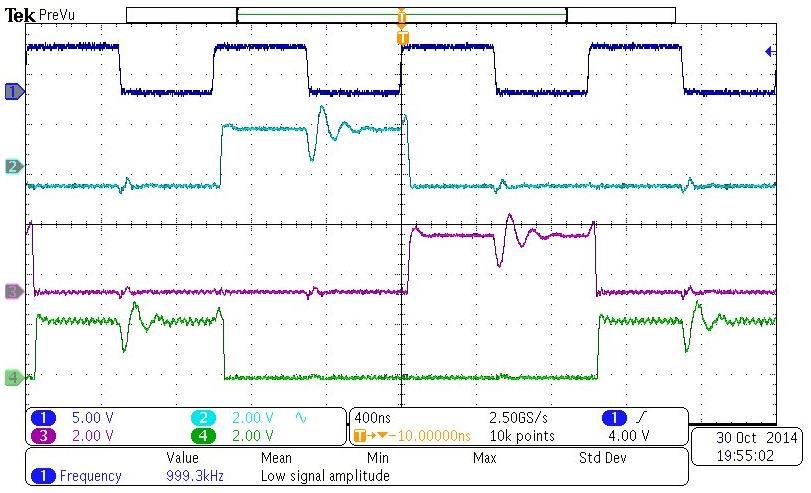
Looking at the measurements once again we see that the delay is actually a bit bigger than the one expected. But nevertheless, the result seems reasonable.

**Part 4: Sequential circuits**

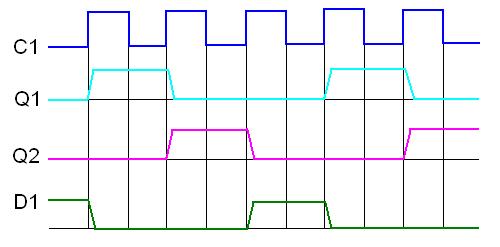
**LAB TASK 4.1**



The circuit shown is implemented using a 74HC175 Quad D-type flip-flop and a 74HC7266 Quad 2-input XNOR device. A function generator is connected to the C1 input and a rectangular signal at 1 MHz is applied to it. Precautions were made to make sure that the signal ranges between 0...5V. In order to reset the D-flip-flops a debounced push button is connected to the C1 input. The 4 signals C1(Channel1), Q1(Channel 2), Q2(Channel 3) and D1(Channel4) are displayed on the oscilloscope.



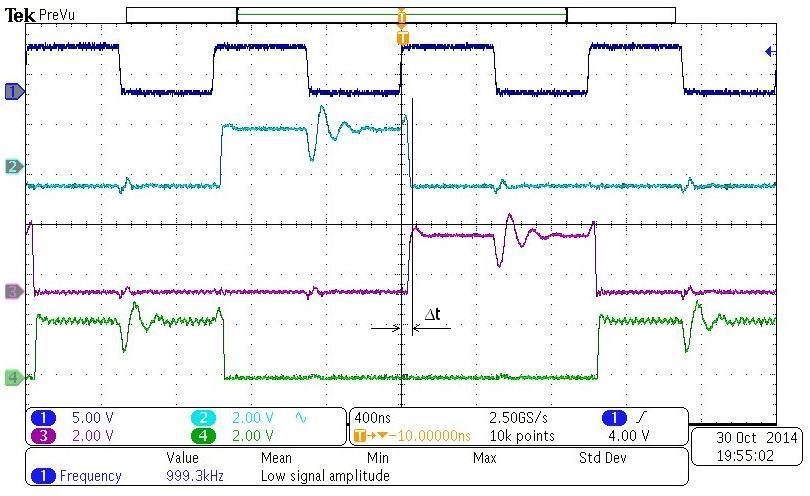
Expected output:



The result is the same as the one expected.

The delay between the rising edge of the clock signal C1 to the change of the output of the flip-flop Q (**∆t** from the pic below) is:

400 ns per unit; ∆t ≈ 1/5 of a unit ≈ 80 ns



The extra task is not done due to lack of time.